REMARKS

Claims 1-10 have been rejected.

Claims 11-17 have been added.

No claims have been allowed.

Claims 2-10 have been amended.

Claims 1-17 are pending in this application.

Reconsideration of the claims of this application is respectfully requested.

I. 35 U.S.C. § 102(e) – Anticipation

The Office Action rejects Claims 1-4 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,233,637 issued to Smyers et al. ("*Smyers*"). This rejection is respectfully traversed.

Smyers recites a system for providing a bi-directional path between an application and a data bus. (*Abstract*). The system includes an isochronous data pipe and an asynchronous data pipe, and each data pipe includes a register set. (*Col. 3, Lines 30-43*). Each data pipe facilitates communication of information between an application (elements 12 and 14) and a bus structure (element 58). (*Col. 3, Lines 32-33*).

Smyers simply recites the use of data pipes to allow an application and a data bus to communicate. Data from an application is transported toward the bus, and data from the bus is transported toward the application. *Smyers* lacks any mention of transferring data between the registers in the data pipes. As a result, *Smyers* fails to disclose, teach, or suggest a "plurality of

register transfer units ... that facilitate transfers of data among interface registers" as recited in Claim 1.

The Office Action asserts that *Smyers* recites this element at column 3, line 64 through column 4, line 7. (*Office Action, Page 3, Second paragraph*). The Applicant respectfully notes that the cited portion of *Smyers* simply recites using First In, First Out (FIFO) queues to facilitate the transport of information between the data pipes and the bus. *Smyers* never discloses, teaches, or suggests that the FIFO queues facilitate the transfer of data between the registers in the data pipes. As a result, the cited portion of *Smyers* fails to disclose, teach, or suggest a "plurality of register transfer units ... that facilitate transfers of data among interface registers" as recited in Claim 1.

For at least these reasons, *Smyers* fails to anticipate Claim 1 (and its dependent claims). The Applicant respectfully requests withdrawal of the § 102(e) rejection and full allowance of Claims 1-4.

II. 35 U.S.C. § 103(a) – Obviousness

The Office Action rejects Claims 5-10 under 35 U.S.C. § 103(a) as being unpatentable over *Smyers* in view of "Applicant Admitted Prior Art" ("*AAPA*"). This rejection is respectfully traversed.

Claim 5 depends from Claim 1. As described above, *Smyers* fails to disclose, teach, or suggest a "plurality of register transfer units ... that facilitate transfers of data among interface registers" as recited in Claim 1. Because Claim 5 depends from an allowable claim, Claim 5 is

patentable.

Regarding Claims 6-10, *Smyers* fails to disclose, teach, or suggest a "plurality of register transfer units" that facilitate "transfers of data among interface registers" as recited in Claim 6. The Office Action only relies on the *AAPA* as reciting a channel decoder. The Office Action does not cite the *AAPA* as reciting a "plurality of register transfer units" that facilitate "transfers of data among interface registers."

For at least these reasons, the proposed *Smyers-AAPA* combination fails to disclose, teach, or suggest Claim 6 (and its dependent claims). The Applicant respectfully requests withdrawal of the § 103(a) rejection and full allowance of Claims 5-10.

III. New Claims

The Applicant has added new Claims 11-17. The Applicant submits that no new matter has been added. The Applicant respectfully requests entry and full allowance of Claims 11-17.

CLAIM AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

2. (Amended) The bridge of claim 1, further **[including]** comprising:

an instruction memory that is configured to contain register transfer instructions, and

wherein the operable coupling of the plurality of register transfer units and the plurality of function units is effected via the register transfer instructions.

3. (Amended) The bridge of claim 1, further **[including]** comprising:

at least one datapath unit, operably coupled to the plurality of register transfer units, that facilitates a transformation of at least one data item of the data that is transferred among the interface registers.

4. (Amended) The bridge of claim 3, further **[including]** comprising:

an instruction memory that is configured to contain register transfer instructions, and

wherein the operable coupling of the plurality of register transfer units and the plurality of function units and the at least one datapath unit is effected via the register transfer instructions.

5. (Amended) The bridge of claim 1, wherein:

at least one of the function units is a programmable digital signal processor.

6. (Amended) A signal processing system comprising:

a receiver that is configured to provide a digital input stream,

a channel decoder, operably coupled to the receiver, that is configured to decode the digital input stream into a decoded signal stream, and

a user application, operably coupled to the channel decoder, that is configured to render an output corresponding to a channel of the digital input stream based on the decoded signal stream,

wherein the channel decoder comprises a bridge comprising:

a plurality of interface registers, each associated with a processing unit of a plurality of processing units, and

a plurality of register transfer units, operably coupled to the plurality of interface registers, that facilitate:

transfers of data among interface registers of the plurality of interface registers,

transfers of data of the digital input stream among interface registers of the plurality of interface registers, and

transfers of data from the interface registers to provide the decoded signal stream.

7. (Amended) The signal processing system of claim 6, wherein the channel decoder further **[includes]** comprises:

an instruction memory that is configured to contain register transfer instructions, and

wherein the operable coupling of the plurality of register transfer units and the plurality of processing units is effected via the register transfer instructions.

8. (Amended) The signal processing system of claim 6, further **[including]** comprising:

at least one datapath unit, operably coupled to the plurality of register transfer units, that facilitates a transformation of at least one data item of the data that is transferred among the interface registers.

9. (Amended) The signal processing system of claim 8, wherein the channel decoder further **[includes]** comprises:

an instruction memory that is configured to contain register transfer instructions, and

wherein the operable coupling of the plurality of register transfer units and the plurality of processing units and the at least one datapath unit is effected via the register transfer instructions.

10. (Amended) The signal processing system of claim 6, wherein:

at least one of the processing units is a programmable digital signal processor.

SUMMARY

For the reasons given above, the Applicant respectfully requests reconsideration and allowance of pending claims and that this application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@davismunck.com.***

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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